

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln Of: NAKAYAMA

Serial No.: 09/593,891

Filed: June 14, 2000

For: SEMICONDUCTOR STORAGE DEVICE

Group: 2815

Examiner: CHU

DOCKET: NEC DP-624

The Assistant Commissioner of Patents  
Washington, D.C., 20231

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AMENDMENT B UNDER RULE 116

FEB 28 2002

TECHNOLOGY CENTER 2800

Dear Sir:

This amendment is being filed in response to the Final Action mailed November 29, 2001. Please amend the application as follows:

IN THE CLAIMS:

Kindly amend claim 1 to read as follows:

1. (Twice Amended) A stacked semiconductor storage device comprising, in combination, a lower chip and an upper chip superimposed on a substrate, said semiconductor storage device further comprising:
- a wiring substrate having wiring patterns thereon, interposed between said lower chip and said upper chip, for relaying electric connection between bonding pads on said upper chip and bonding pads on said substrate, wherein the bonding pads on said upper chip are arranged in a line running perpendicular to a line of bonding pads on the substrate.

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February 28, 2002

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MESSAGE: RE: NAKAYAMA  
U.S. Patent Appln. serial No. 09/593,891  
Filed: June 14, 2000  
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Our Ref: NEC DP-624

Enclosure: Amendment B Under Rule 116 w/Marked Copy of Amended Claim

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